REMARKS

Claims 1-33 were pending in this application.

Claims 1-33 have been rejected.

Claims 1-33 have been amended as shown above.

Claims 1-33 remain pending in this application.

Reconsideration and full allowance of Claims 1-33 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 112

The Office Action rejects Claims 1-33 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. In particular, the Office Action asserts that the use of the terms "K", "K+1", and "N" is confusing.

The Applicants have amended Claims 1-33 to remove the term "N". The Applicants have also amended Claims 1-33 to replace the terms "K", "K+1", "K-1", and "K+2" with the terms "first", "second", "third", and "fourth", respectively. The Applicants respectfully note that the terms "first", "second", "third", and "fourth" do not imply any particular order of delay cells or refer to particular delay cells. Rather, these terms are used to distinguish between different delay cells.

The Applicants respectfully submit that Claims 1-33 are definite and distinctly claim the subject matter regarded as the invention. Accordingly, the Applicants respectfully request withdrawal of the § 112 rejection.

II. REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-33 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,130,565 to Nagano et al. ("*Nagano*"). The Applicants respectfully traverse this rejection.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

Nagano recites a phase locked loop (PLL) that includes a phase difference comparison circuit 202, a charge pump circuit 102, a filter 304, and a voltage controlled oscillation circuit 402. (*Figure 18; Col. 23, Line 67 – Col. 24, Line 4*). The oscillation circuit 402 includes a control circuit 4020 and multiple delay circuits 40201 through 40233. (*Figure 19; Col. 24, Lines 32-35*). The output of the first delay circuit 40201 and the output of the last delay circuit 40233 are provided to the phase difference comparison circuit 202. (*Figure 19; Col. 27, Lines 2-9*). The phase difference comparison circuit 202 generates "up" or "down" currents based on a comparison of its two inputs. (*Col. 24, Lines 5-8*).

First, Claims 1, 12, and 23 recite monitoring "outputs of at least a first delay cell and a second delay cell immediately following the first delay cell." The cited portions of *Nagano* recite that the outputs of first and last "delay circuits" are provided to a phase difference

comparison circuit 202. The cited portions of *Nagano* do not recite that the outputs of two consecutive delay circuits are provided to the phase difference comparison circuit 202. As a result, the cited portions of *Nagano* fail to anticipate monitoring "outputs of at least a first delay cell and a second delay cell immediately following the first delay cell" as recited in Claims 1, 12, and 23.

Second, Claims 1, 12, and 23 recite determining that a "clock edge" has "reached an output of [the] first delay cell and has not reached an output of [the] second delay cell" and generating a "control signal" capable of adjusting the power supply level based on the determination. The cited portions of *Nagano* simply recite that the outputs of first and last "delay circuits" are provided to a phase difference comparison circuit 202, which produces a current based on a comparison of the delay circuits' outputs. The cited portions of *Nagano* lack any mention that the phase difference comparison circuit 202 adjusts a power supply level based on a determination that a "clock edge" has reached the output of one delay circuit but not the output of the next consecutive delay circuit. As a result, the cited portions of *Nagano* fail to anticipate determining that a "clock edge" has "reached an output of [the] first delay cell and has not reached an output of [the] second delay cell" and generating a "control signal" capable of adjusting the power supply level "based on the determination" as recited in Claims 1, 12, and 23.

For these reasons, the cited portions of *Nagano* fail to anticipate the Applicants' invention as recited in Claims 1, 12, and 23 (and their dependent claims).

The dependent claims are patentable over the cited portions of *Nagano* due to their dependence from allowable base claims and in light of their own recitations. For example,

Claims 6, 7, 17, 18, 28, and 29 recite monitoring outputs of a "third delay cell immediately preceding the first delay cell" and a "fourth delay cell immediately following the second delay cell." As described above, the cited portions of *Nagano* simply recite processing outputs of first and last "delay circuits." The cited portions of *Nagano* lack any mention of monitoring the outputs of four different delay circuits. The Office Action makes no attempt to show how the cited portions of *Nagano* anticipate these elements of Claims 6, 7, 17, 18, 28, and 29.

As another example, Claims 8-11, 19-22, and 30-33 recite altering a power supply level in relatively large or relatively small "incremental steps." The cited portions of *Nagano* lack any mention of adjusting a power supply level in larger and smaller incremental steps. The Office Action makes no attempt to show how the cited portions of *Nagano* anticipate these elements of Claims 8-11, 19-22, and 30-33.

Accordingly, the Applicants respectfully request withdrawal of the § 102 rejection and full allowance of Claims 1-33.

III. CONCLUSION

As a result of the foregoing, the Applicants assert that all claims in this application are in condition for allowance and respectfully request an early allowance of such claims.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: Dec. 22, 2004

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